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What is claimed is:

1. A method for managing memory in a network switch, said method comprising the steps of:

providing a memory, wherein the memory includes a plurality of memory locations configured to store data therein;

providing a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location;

providing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool;

reading available memory addresses from the memory address pool using a last in first out operation;

writing released memory addresses into the memory address pool; and

adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool.

2. A method for managing memory in a network switch as recited in claim 1, wherein the steps of reading available memory addresses and writing released memory addresses are initiated during a second clock cycle when the reading step and the writing step are requested in a first clock cycle.

3. A method for managing memory in a network switch, said method comprising the steps of:

receiving a request from a module for a next available memory address in a first clock cycle;

receiving a released memory address in the first clock cycle; and

passing off the released memory address to the module requesting the next available memory address in a second clock cycle.

4. A method for managing memory in a network switch as recited in claim 3, wherein the passing off step operates without incrementing or decrementing a next available memory address pointer.

5. A method for managing memory, said method comprising the steps of:

providing a memory having a predetermined number of memory storage

locations therein;

providing a predetermined number of addresses in a stack, each of the predetermined number of addresses corresponding to a unique memory storage location; and

providing an address pointer for indicating a next available address to be used from the predetermined number of addresses in the stack, wherein the address pointer releases an address in a last-in first-out type operation.

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6. A method for managing memory as recited in claim 5, wherein the method further comprises the step of passing off an address released back to the stack to a request for an available address when a release of an address beck to the stack occurs in the same clock cycle as the request for an available address.

7. A method for managing memory as recited in claim 6, wherein the method further comprises passing off the address released without incrementing or decrementing the address pointer.

8. An apparatus for managing memory in a network switch, said apparatus comprising:

a memory address pool having a plurality of memory addresses, each of said plurality of memory addresses corresponding to an individual memory location in a memory; and

a memory controller in connection with said memory and said memory address pool,

wherein said memory controller manages an address pointer for indicating a next available memory address in said memory address pool.

9. An apparatus for managing memory in a network switch as recited in claim 8, wherein said memory address pool further comprises a cell free address pool.

10. An apparatus for managing memory in a network switch as recited in claim 8, wherein said memory address pool further comprises a slot free address pool.

11. An apparatus for managing memory in a network switch as recited in claim 8, wherein said memory controller is further configured to read an available memory address from said memory address pool and to write a released memory address ~~to said address pool.~~

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12. An apparatus for managing memory in a network switch as recited in claim 11, wherein said memory controller is further configured to read said available memory address and write said released memory address in the same clock cycle without adjusting said address pointer.

13. An apparatus for managing memory in a network switch, said apparatus comprising:

a memory address pool in connection with said memory, said memory address pool having a predetermined number of memory addresses therein, each of said predetermined number of memory addresses corresponding to an individual memory location in a memory; and

a memory controller in connection with said memory and said memory address pool,

wherein said memory controller passes off a released memory address to a request for an available memory address when a request for said available address is received during the same clock cycle as said released memory address is released.

14. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory further comprises SDRAM.

15. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory further comprises SRAM.

16. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory address pool further comprises a cell free address pool.

17. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory address pool further comprises a slot free address pool.

18. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory controller further comprises a common buffer pool controller.

19. An apparatus for managing memory in a network switch as recited in claim 13, wherein said memory controller further comprises a SDRAM controller.

20. An apparatus for managing memory in a network switch, said apparatus comprising:

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a memory, wherein the memory includes a plurality of memory locations configured to store data therein;

a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location;

means for managing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool;

means for reading available memory addresses from the memory address pool using a last in first out operation;

means for writing released memory addresses into the memory address pool; and

means for adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool,

wherein said means for reading and said means for writing are configured to pass off an available memory address when a request to read an address is received during the same clock cycle as a request to write an address.